	Search Terms
1	CARLOS-VINCENT-J
2	DORAN-JAMES-E
3	FOCU
4	FOCUS
5	KNIGHT-STEPHEN-E
6	LEIDY-ROBERT-K
7	MACHIA-KEITH-J
8	RESIST
9	SHAVER-JOSEPH-E
10	SUNDLING-DIANNE-L
11	RESISTS
12	(((((((((BOWLEY-REGINALD-R.IN.) OR (CARLOS-VINCENT-J.IN.)) OR (DORAN-JAMES-E.IN.)) OR (SHAVER-JOSEPH-E.IN.)) OR (MACHIA-KEITH-J.IN.)) OR (SUNDLING-DIANNE-L.IN.)) OR (KNIGHT-STEPHEN-E.IN.)) OR (LEIDY-ROBERT-K.IN.)) AND FOCUS AND RESIST)

	Total	USPAT	US-PGPUB	EPO	JPO	Derwent	IBM TDB	USOCR
1	1							
2	1							
3	65							
4	243173							
5	5							
6	39							
7	2							
8	296997							
9	1							
10	2							
11	72739							
12	20	17	3	0	0	0	0	

	U	1	Document ID	Issue Date	Pages	Title	Current OR
1	☐	☐	US 20030158710 A1	20030821	26	Contact hole profile and line edge width metrology for critical image control and feedback of lithographic focus	702/189
2	☒	☐	US 20030091907 A1	20030515	7	Reverse tone process for masks	430/5
3	☒	☐	US 20010021577 A1	20010913	44	METHOD FOR FORMING SIDEWALL SPACERS USING FREQUENCY DOUBLING HYBRID RESIST AND DEVICE FORMED THEREBY	438/595
4	☒	☐	US 6420766 B1	20020716		Transistor having raised source and drain	257/401
5	☒	☐	US 6303416 B1	20011016		Method to reduce plasma etch fluting	438/166
6	☒	☐	US 6278515 B1	20010821		Method and apparatus for adjusting a tilt of a lithography tool	355/55
7	☒	☐	US 6255178 B1	20010703		Method for forming transistors with raised source and drains and device formed thereby	438/300
8	☒	☐	US 6232639 B1	20010515		Method and structure to reduce latch-up using edge implants	257/372
9	☒	☐	US 6218704 B1	20010417		ESD protection structure and method	257/355

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1			Bowley, Reginald R. JR. et al.	☒	☐	☐	☐	☐	☐	☐	US 20030158710	☐
2	430/322; 430/324		Horak, David V. et al.	☐	☐	☐	☐	☐	☐	☐	US 20030091907	☐
3	257/E21.027; 257/E21.252; 257/E21.257; 257/E21.435; 257/E21.437		BROWN, JEFFREY S. et al.	☐	☐	☐	☐	☐	☐	☐	US 20010021577	☐
4	257/327; 257/622; 257/E21.027; 257/E21.252; 257/E21.257; 257/E21.435; 257/E21.437		Brown, Jeffrey S. et al.	☐	☐	☐	☐	☐	☐	☐	US 6420766	☐
5	438/942		Bruce, James A. et al.	☐	☐	☐	☐	☐	☐	☐	US 6303416	☐
6	250/216; 250/492.2; 250/492.22; 355/53; 355/77; 430/30; 430/311; 430/314; 430/4		Knight, Stephen E. et al.	☐	☐	☐	☐	☐	☐	☐	US 6278515	☐
7	257/E21.027; 257/E21.252; 257/E21.257; 257/E21.435; 257/E21.437; 438/303		Brown, Jeffrey S. et al.	☐	☐	☐	☐	☐	☐	☐	US 6255178	☐
8	257/519; 257/E21.642; 257/E27.063		Baker, Faye D. et al.	☐	☐	☐	☐	☐	☐	☐	US 6232639	☐
9	257/356; 257/358; 257/359; 257/546; 257/E29.063		Brown, Jeffrey S. et al.	☐	☐	☐	☐	☐	☐	☐	US 6218704	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
10	☒	☐	US 6184151 B1	20010206	26	Method for forming cornered images on a substrate and photomask formed thereby	438/743
11	☒	☐	US 6147394 A	20001114	43	Method of photolithographically defining three regions with one mask step and self aligned isolation structure formed thereby	257/506
12	☒	☐	US 6100013 A	20000808	43	Method for forming transistors with raised source and drains and device formed thereby	430/312
13	☒	☐	US 6033949 A	20000307	37	Method and structure to reduce latch-up using edge implants	438/232
14	☒	☐	US 5981148 A	19991109	41	Method for forming sidewall spacers using frequency doubling hybrid resist and device formed thereby	430/314
15	☒	☐	US 5976768 A	19991102	40	Method for forming sidewall spacers using frequency doubling hybrid resist and device formed thereby	430/314

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
10	257/E21.035; 257/E21.036; 257/E21.652; 438/717; 438/736; 438/737; 438/738; 438/744		Adair, William J. et al.	☐	☐	☐	☐	☐	☐	☐	US 6184151	☐
11	257/641; 257/649; 257/E21.545		Bruce, James A. et al.	☐	☐	☐	☐	☐	☐	☐	US 6147394	☐
12	216/46; 257/E21.027; 257/E21.252; 257/E21.257; 257/E21.435; 257/E21.437; 430/314; 430/317; 438/303		Brown, Jeffery S. et al.	☐	☐	☐	☐	☐	☐	☐	US 6100013	☐
13	148/DIG.137; 257/E21.642; 257/E27.063; 438/223; 438/227		Baker, Faye D. et al.	☐	☐	☐	☐	☐	☐	☐	US 6033949	☐
14	257/E21.027; 257/E21.252; 257/E21.257; 257/E21.435; 257/E21.437; 430/312; 430/313; 430/316; 438/696		Brown, Jeffrey S. et al.	☐	☐	☐	☐	☐	☐	☐	US 5981148	☐
15	257/E21.027; 257/E21.252; 257/E21.257; 257/E21.435; 257/E21.437; 430/316; 430/394; 438/445; 438/447; 438/696		Brown, Jeffrey S. et al.	☐	☐	☐	☐	☐	☐	☐	US 5976768	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
16	☒	☐	US 5972570 A	19991026	44	Method of photolithographically defining three regions with one mask step and self aligned isolation structure formed thereby	430/314
17	☒	☐	US 5959325 A	19990928	27	Method for forming cornered images on a substrate and photomask formed thereby	257/302
18	☒	☐	US 5939767 A	19990817	36	Structure and process for buried diode formation in CMOS	257/551
19	☒	☐	US 5882967 A	19990316	36	Process for buried diode formation in CMOS	438/237
20	☒	☐	US 5861330 A	19990119	37	Method and structure to reduce latch-up using edge implants	438/232

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
16	257/E21.545; 430/313; 430/317		Bruce, James A. et al.	☐	☐	☐	☐	☐	☐	☐	US 5972570	☐
17	257/E21.035; 257/E21.036; 257/E21.652; 438/387; 438/942		Adair, William J. et al.	☐	☐	☐	☐	☐	☐	☐	US 5959325	☐
18	257/355; 257/481; 257/603; 257/E21.632		Brown, Jeffrey S. et al.	☐	☐	☐	☐	☐	☐	☐	US 5939767	☐
19	257/E21.632; 430/270.1; 430/325; 430/326; 438/200; 438/526		Brown, Jeffrey S. et al.	☐	☐	☐	☐	☐	☐	☐	US 5882967	☐
20	257/E21.642; 257/E27.063; 430/311; 438/223; 438/227; 438/529		Baker, Faye D. et al.	☐	☐	☐	☐	☐	☐	☐	US 5861330	☐